METHOD AND CIRCUIT FOR ADJUSTING THE TIMING OF OUTPUT DATA BASED ON THE CURRENT AND FUTURE STATES OF THE OUTPUT DATA

ABSTRACT OF THE DISCLOSURE

A clock synchronization circuit receives an input clock signal along with current and future data signals. The clock synchronization circuit generates a phase shifted clock signal in response to the input clock signal, with the phase shifted clock signal having a phase shift relative to the input clock signal that is a function of the current and future data signals. The clock synchronization circuit may also generate a plurality of phase shifted clock signals, with each phase shifted clock signal having a respective phase shift that is a function of the current and future logic states of groups of the other data signals.